International Journal of Engineering Science Invention Research & Development; Vol. I Issue XI May 2015
www.ijesird.com e-ISSN: 2349-6185

Implementation of CORDIC on FPGA using VHDL to compare word serial & pipelined architecture.

Mohd Ahmer[1], Mohammad Haris Bin Anwar[2], Amsal Subhan[3]
Lecturer[1], Lecturer[2] M.Tech. Student[3] Department of Electronics and Communication, Engineering, Integral University Lucknow.
[1]mahmer@iul.ac.in, [2]mhdanwar@iul.ac.in, [3]amsal2009@gmail.com

***Abstract*: - The CORDIC abbreviated as Coordinate Rotation Digital Computer was first described in 1959 by J. E Volder [1]. This paper deals with some of the CORDIC architectures and their comparison on different aspects like power, speed and number of components to make it easy for the software programmers to select as per their need. The two architectures of CORDIC i.e. word serial and pipelined architecture have been programmed through VHDL on Xilinx 8.1. The interesting fact got in the result is that word serial architecture offers a low cost because it requires fewer resources, whereas pipelined architecture offers high speed and accuracy at the cost of increased resources.**

***Keywords*— Xilinx, FPGA, CORDIC and VHDL.**

I. INTRODUCTION

CORDIC also known as the digit-by digit method and Volder's algorithm, is a simple and efficient algorithm to calculate trigonometric and hyperbolic functions.The CORDIC has been used in simple calculators to complex communication system to calculate various functions such as trigonometric, logarithmic, and hyperbolic and various other functions. The research on CORDIC has developed various architectures of it which are implemented to utilize it for various purpose. But the complexity lies in for a programmer to choose which architecture for its system. It is commonly used when no hardware multiplier is available. It only requires addition, subtraction, bit shift and table look-up.

The CORDIC algorithm has found its way into diverse applications including the 8087 math coprocessor, the HP-35 calculator, radar signal and robotic [2]. CORDIC rotation has also been proposed for computing Discrete Fourier, Discrete Cosine, and Singular value Decomposition [3], image compression [5] and solving linear systems [1].

II. CORDIC ALGORITHM

CORDIC is a special purpose digital computer for real time computations. This algorithm was specially developed for real time digital computers where the majority of computations involved trigonometric relationships. It contains special arithmetic unit consisting of shift registers, adder–subtractors and special interconnects. CORDIC algorithm was first proposed by Jack Volder in 1959[1]. This algorithm is derived from general rotation transform

$$x'=x*\cos\emptyset - y*\sin\emptyset \ldots\ldots\ldots (1)$$

$$y'=y*\cos\emptyset + x*\sin\emptyset \ldots\ldots\ldots (2)$$

Which rotates a vector in Cartesian form? The above two equations can be modified as

$$x'=\cos\emptyset x - y*\tan\emptyset \ldots\ldots (3)$$

$$y'=\cos\emptyset y + x*\tan\emptyset \ldots\ldots (4)$$

If the rotation is restricted to tan (φ) = +/- 2(-i), the multiplication in the above equation will be replaced by simple shift operation. The rotation can now be expressed as

$$Xi+1=KiXi - Yi*di*2 - i \ldots (5)$$

$$Yi+1=KiYi + Xi*di*2 - i \ldots. (6)$$

Where i is the iteration count and

$$Ki=\cos\tan{-1}\ 2-i \ldots\ldots (7)$$

And di = +/- 1.

Removing the scaling factor the iteration equation is simple shift and add equation. The value of K approaches to 0.607 as the iteration count approaches infinity. The direction in which the vector should be rotated is given by the equation

$$Zi+1= Zi - di*\tan{-1}\ 2-i \ldots. (8)$$

Where $di= -1\ if Zi<0,+1\ otherwise.$

J.S.Walther modified the equation given by Volder. His modification to the original CORDIC equations helped calculating hyperbolic and linear functions [5]. He proposed generalized equation which can be used to calculate functions belonging to all three

coordinate systems. He considered coordinate system parameterized by „m" . The modified equations are as given

$$Xi+1 = Xi - m*Yi*di*2 \ldots\ldots (9)$$

$$Yi+1 = Yi + Xi*di*2 - i \ldots\ldots\ldots (10)$$

$$Zi+1 = Zi - di*Ei \ldots\ldots\ldots\ldots (11)$$

WHERE $di = -1\ if Zi<0, +1\ otherwise.$

III. CORDIC ARCHITECTURES

CORDIC has following architectures illustrated in below figure which are classified as Folded and unfolded [4]. Further Folded has two architectures Bit Serial and Word Serial, and Unfolded too had two architectures Parallel and Pipelined architecture:-

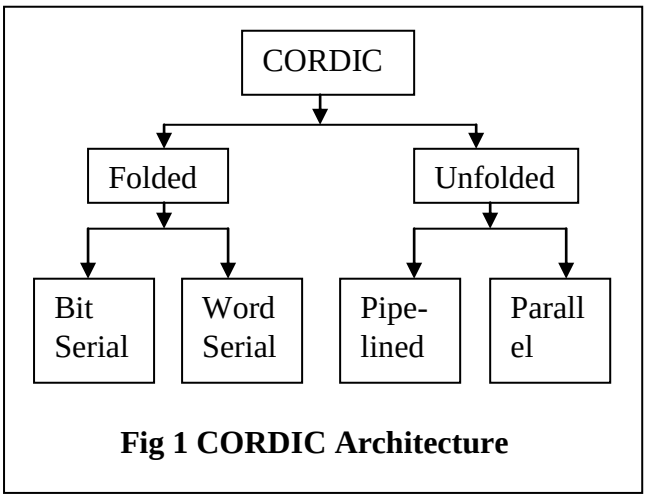


Fig 1 CORDIC Architecture

1) **Folded Word Serial Architecture:** -A folded world serial design is also known as iterative bit-parallel design [6] which is obtained simply by duplicating each of the three difference equation shown in hardware.

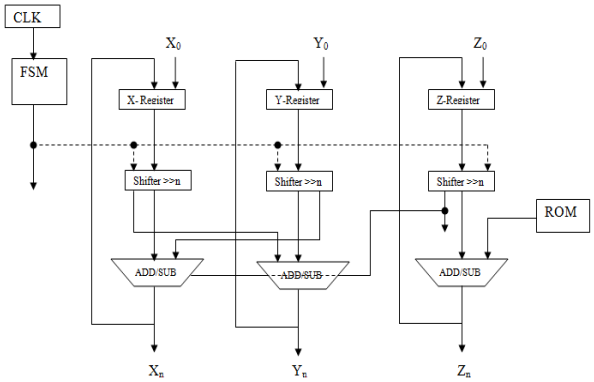


Figure 2 Folded Word serial Architecture

Unfolded Pipelined Architecture

The iterative nature of the CORDIC processor discussed above demands that the processor has to perform iterations at n times the data rate [7].The iteration process can be unfolded so that each of n processing elements always performs the same iteration [8]. A direct application of the unfolding transformation is to design parallel processing architectures from serial processing architectures. An unfolded CORDIC processor is shown in figure.

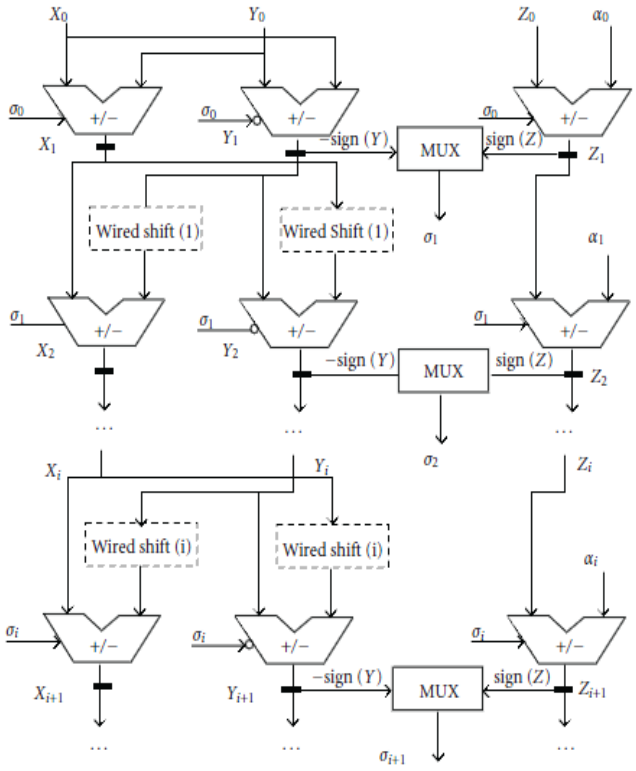


Figure 3 Unfolded Parallel Architecture

VHDL Implementation: -The CORDIC algorithm is based on mainly three components: controlled shift registers, adders and subtractors[9]. The CORDIC algorithm has been designed using three blocks and other components as required in VHDL. All the components used are designed individually in VHDL and finally using the structural mode of styling, interfacing among all the components is completed.

IV. RESULT

Simulation Result for Word Serial Architecture: -Below figure 4 shows external RTL of CORDIC (16 bit word Serial Architecture), figure 5shows internal RTL.

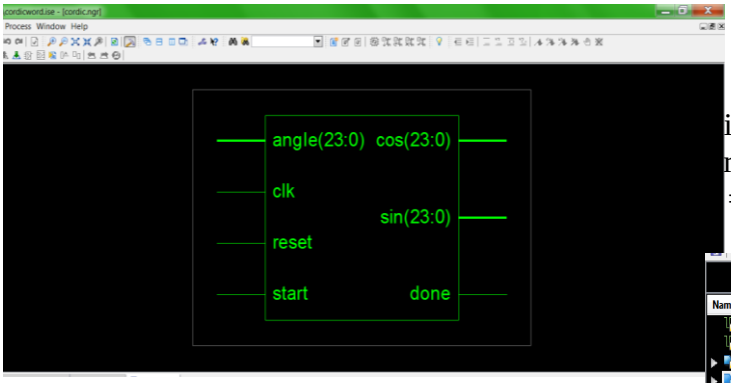


Figure 4 External RTL of CORDIC (Word Serial Architecture)

Figure 6 illustrates the simulation result for 60 degree(430548 H). It shows sin = 376CF9 (H) and cos = 200003(H).

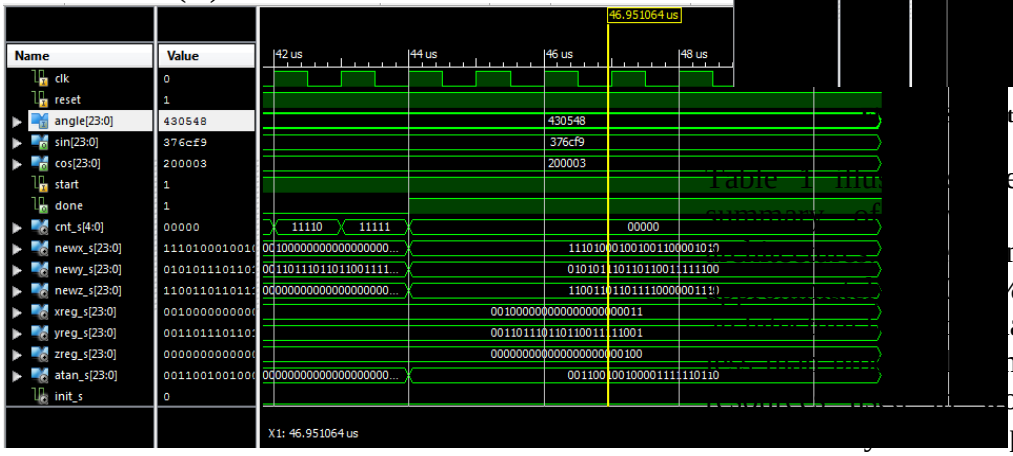


Figure 5 Simulation result for 60° angle

Simulation Results for Pipelined Architecture

Below figure7 shows external RTL of CORDIC (16 bit Pipelined Architecture), figure 8 shows internal RTL.

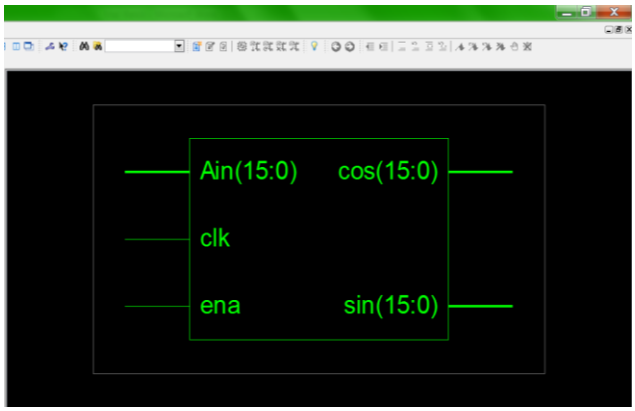
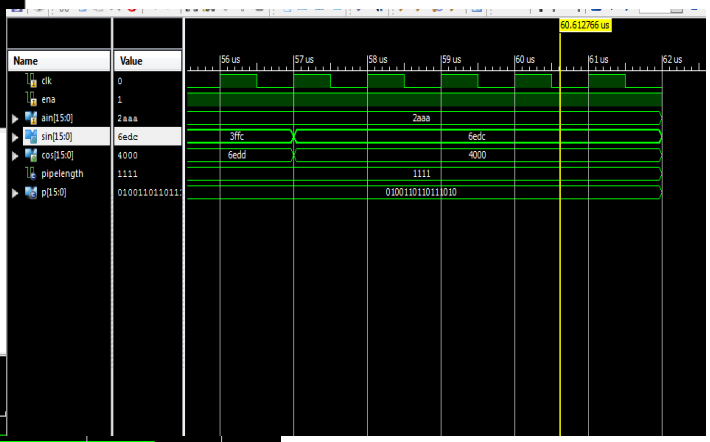


Figure 6 External RTL of CORDIC (Pipelined Architecture)

igure 7 illustrates the simulation result for 60 ree (2AAA H). It shows sin = 6EDC (H) and = 4000 (H).



tion result for 60° angle

e comparison between the Utilization in both the mber of bonded IOBs is % more than pipelined ardware resources are much itecture. Hence, the overall rd serial architecture are pipelined architecture. From below table it is clear that word serial architecture utilizes less hardware in comparison to the

pipelined architecture. As the number of resources utilized in word serial architecture are less hence, it can be said that word serial resources has less power utilization in comparison to the pipelined architecture.

Table 1 Comparison of Device summary

DEVICE UTILIZATION SUMMARY						
	Word Serial CORDIC			Pipelined CORDIC		
Logic Utilization	Used	Available	Utilization	Used	Available	Utilization
No. of Slices	235	2352	9%	397	2352	16%
No. of Slice FFs	115	4704	2%	745	4704	15%
No. of 4 i/p LUTs	383	4704	8%	725	4707	15%
No. of bonded IOBs	75	284	26%	50	288	17%
No. of GCLKs	1	4	25%	1	4	25%

Table 2 Angles computed from both the architectures

Computed angles of both the architectures				
Angle	Word Serial Architecture (24 bit)			
	0º	30º	45º	60º
Sin	000000 H	2000003 H	2D413A H	376CF9 H
Cos	400000 H	376CF9 H	296584 H	07CCB4 H
Angle	Pipelined Architecture (16 bit)			
	0º	30º	45º	60º
Sin	01CC H	3FFC H	5A82 H	6EDC H
Cos	8000 H	6EDD H	5A83	4000 H

Table 2 shows a summary of angles computed by both the architectures i.e. word serial and pipelined architecture. As word serial word serial architecture utilizes iteration hence, it is less accurate and if the number of bits are increased then it takes more time to calculate. Whereas pipelined architecture is more accurate and does not suffer such problem.

V. CONCLUSION

The CORDIC algorithm has found its way into diverse application including the 8087 math coprocessor, the HP-35 calculator [7], radar signal processors and robotics. CORDIC rotation has also been proposed for computing Discrete Fourier, Discrete Cosine, Singular value decomposition [9].CORDIC Word Serial Architecture offers low Cost in comparison with pipelined architecture as it utilizes less resources. Hence these finds application in math Processor and handheld calculators where low cost is primary requirement. Whereas, Pipelined architecture finds application in navigation devices used in ships and air-planes due to its high speed and accuracy.

REFERENCES

[1] Volder, J. (1959). The CORDIC Trigonometric Computing Technique. *IRE Transactions on Electronic Computing*(8), 330-334.

[2] Butner, Y. W. (1987). A new architecture for robot control. *IEEE International Conference on Robotics and Automation*, 664-670.

[3] Banerjee, A. S. (2001). FPGA realization of a CORDIC based FFT processor for biomedical signal processing. *Microprocessors and Microsystems*, 131–142.

[4] Pramod K. Meher, J. V.-B. (2009). 50 Years of CORDIC:Algorithms, Architectures and Applications. *IEEE*.

[5] S. Sathyanarayana, S. R. (2007). Unified CORDIC based processor for image processing. *International Conference on Digital Signal Processing, 15*, 343-346

[6] Jean-Claude Bajard, S. K.-M. (1994). BKM: A New Hardware Algorithm. *IEEE, 43*(8), 955-963.

[7] D. S. Cochran (1997). Algorithm & accuracy in the HP 35, Hewlwtt-Packard Journal, 23, 10.

[8] Meggitt, J. E. (1962). Pseudo division and pseudo multiplication processes. *IBM Journal, 6*, 210–226.

[9] D. F. (1998). A high-speed processor for digital sine/cosine generation and angle rotation. *Conference Record of the Thirty-Second Asilomar Conference on Signals, Systems & Computers*,, 177-181.